BRCM24C04SC SOP-8 4 Kbit I²C

The BRCM24C04SC is 4Kbit I²C-compatible Serial EEPROM (Electrically Erasable Programmable Read-Only Memory) device in a SOP-8 Plastic Package. HF Product Code.

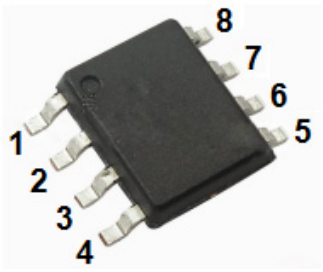
1.7V 2.5~5.5V 1Mhz 1.7~2.5V
400Khz
CMOS 400uA 1.6mA

16

128
5ms
100 100 ESD HBM 6KV
+/-200mA;

Single Supply Voltage
Minimum operating voltage down to 1.7V 1 MHz clock from 2.5V to 5.5V 400kHz clock from 1.7V to 2.5V
Low power CMOS technology Read current 400uA, maximum Write current 1.6mA, maximum
Schmitt Trigger, Filtered Inputs for Noise Suppression
Sequential & Random Read Features
16-byte Page Write Modes
Write protect of the whole memory array
Additional Write Lockable Page and 128-bit Serial Number
Self-timed Write Cycle (5ms maximum)
High Reliability Endurance: > 1 Million Write Cycles Data Retention: > 100 Years HBM: 6KV
Latch up Capability: +/-200mA;

Household appliances, Network communications, Portable Bluetooth devices, Set-top boxes, Smart meters, Fingerprint unlocking devices



| Pin | Name | Type | Description |
|---|---|---|---|
| 1 | NC | - | |
| 2 | E1 | Input | |
| 3 | E2 | Input | |
| 4 | GND | Ground | |
| 5 | SDA | I/O | / |
| 6 | SCL | Input | |
| 7 | WCB | Input | |
| 8 | VCC | Power | |

/ See Marking Instructions

| Parameter | Symbol | Rating | Unit |
|---|---|---|---|
| Storage Temperature | $T_{stg}$ | -65~+150 | |
| Operation Temperature | $T_{opr}$ | -40~+85 | |
| Maximum Operation Voltage | $V_{cc}$ | 6.25 | V |
| Voltage on Any Pin with Respect to Ground | $V_{pin}$ | -1.0~ Vcc+1.0 | V |
| DC Output Current | $I_{out}$ | 5.0 | mA |
| Electro-Static discharge HBM mode | ESD | 6000 | V |

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Endurance | EDR | 25 3.3V Page mode | 1,000,000 | | | Write cycles |
| Data retention | DRET | | 100 | | | Years |

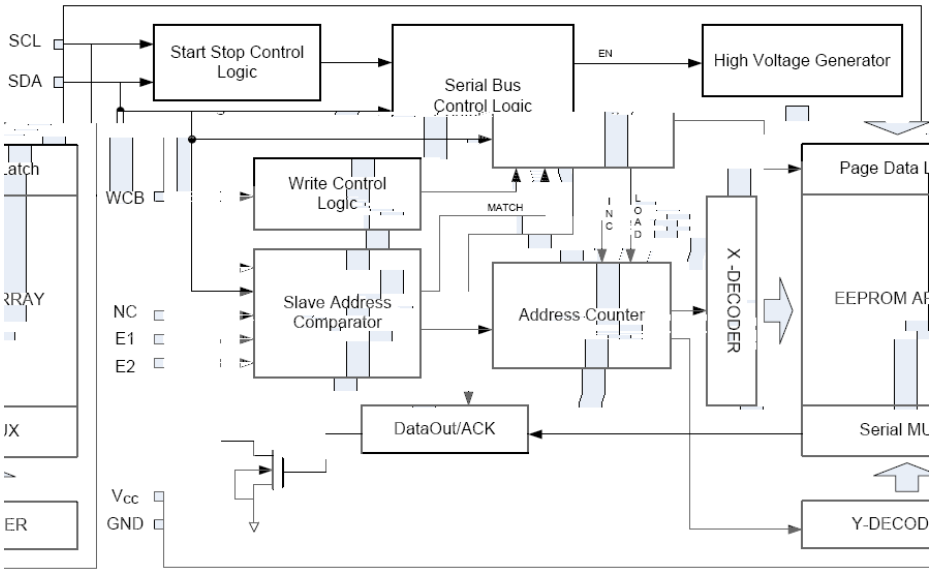
| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Supply Voltage | Vcc | | 1.7 | | 5.5 | V |
| Standby Current | Isb | Vcc = 3.3V, TA = 85°C | | | 1.0 | uA |
| | | Vcc = 5.5V, TA = 85°C | | | 3.0 | uA |
| Supply Current | Icc1 | Vcc=5.5V, Read at 400Khz | | 0.2 | 0.4 | mA |
| Supply Current | Icc2 | Vcc=5.5V,Write at 400Khz | | 0.8 | 1.6 | mA |
| Input Leakage Current | ILI | VIN = Vcc or GND | | 0.1 | 1.0 | uA |
| Output Leakage Current | ILO | VOUT = Vcc or GND | | 0.05 | 1.0 | uA |
| Input Low Level | VIL | | 0.6 | | 0.3Vcc | V |
| Input High Level | VIH | | 0.7Vcc | | Vcc+0.5 | V |
| Output Low Level Vcc = 1.7V (SDA) | VOL1 | IOL = 1.5 mA | | | 0.2 | V |
| Output Low Level Vcc= 3.0V (SDA) | VOL2 | IOL = 2.1 mA | | | 0.4 | V |

| Parameter | Symbol | 1.7V≤Vcc<2.5V | | | 2.5V≤Vcc≤5.5V | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Clock Frequency, SCL | $f_{SCL}$ | - | - | 400 | - | - | 1000 | kHz |
| Clock Pulse Width Low | $t_{LOW}$ | 1.3 | - | - | 0.4 | - | - | us |
| Clock Pulse Width High | $t_{HIGH}$ | 0.6 | - | - | 0.4 | - | - | us |
| Clock Low to Data Out Valid | $t_{AA}$ | 0.05 | - | 0.9 | 0.05 | - | 0.55 | us |
| Noise Suppression Time | $t_I$ | - | - | 0.1 | - | - | 0.05 | us |
| Time the bus must be free before a new transmission can start | $t_{BUF}$ | 1.3 | - | - | 0.5 | - | - | us |
| Start Hold Time | $t_{HD.STA}$ | 0.6 | - | - | 0.25 | - | - | us |
| Start Setup Time | t | | | | | | | |

| Parameter | Symbol | 1.7V≤Vcc<2.5V | | | 2.5V≤Vcc≤5.5V | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Data In Hold Time | $t_{HD.DAT}$ | 0 | - | - | 0 | - | - | us |
| Data In Setup Time | $t_{SU.DAT}$ | 0.1 | - | - | 0.1 | - | - | us |
| Inputs Rise Time[1] | $t_R$ | - | - | 0.3 | - | - | 0.3 | us |
| Inputs Fall Time[1] | $t_F$ | - | - | 0.3 | - | - | 0.1 | us |
| Stop Setup Time | $t_{SU.STO}$ | 0.6 | - | - | 0.25 | - | - | us |
| Data Out Hold Time | $t_{DH}$ | 0.05 | - | - | 0.05 | - | - | us |
| WCB pin Setup Time | $t_{SU.WCB}$ | 1.2 | - | - | 0.6 | - | - | us |
| WCB pin Hold Time | $t_{HD.WCB}$ | 1.2 | - | - | 0.6 | - | - | us |
| Write Cycle Time | $t_{WR}$ | - | - | 5 | - | - | 5 | ms |

Notes:AC measurement conditions:

1. RL (connects to Vcc): 1.3k (2.5V, 5.5V), 10k (1.7V)
2. Input pulse voltages: 0.3 Vcc to 0.7 Vcc
3. Input rise and fall times: ≤50ns
4. Input and output timing reference voltages: 0.5Vcc



p

SDA SDA SCL ( 1 ) SCL
SDA ( 1 )

The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (see to Figure 1). Data changes during SCL high periods will indicate a start or stop condition as defined below.

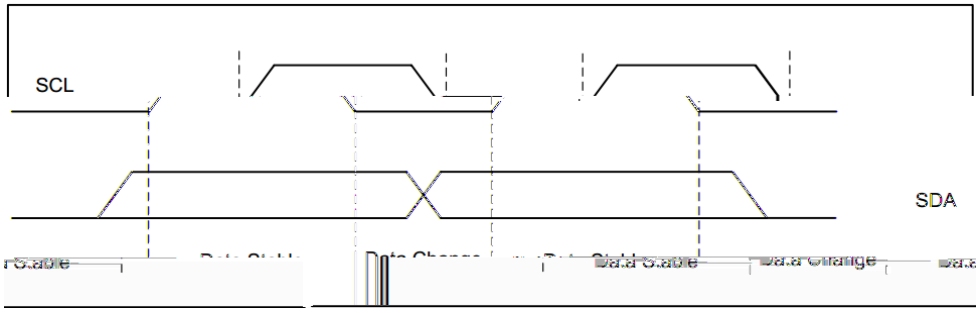



Figure 1 Data Validity

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SCL SDA
2

A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (see to Figure 2).

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SCL SDA
BRCM24C04SC

A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the BRCM24C04SC in a standby power mode (see Figure 2).

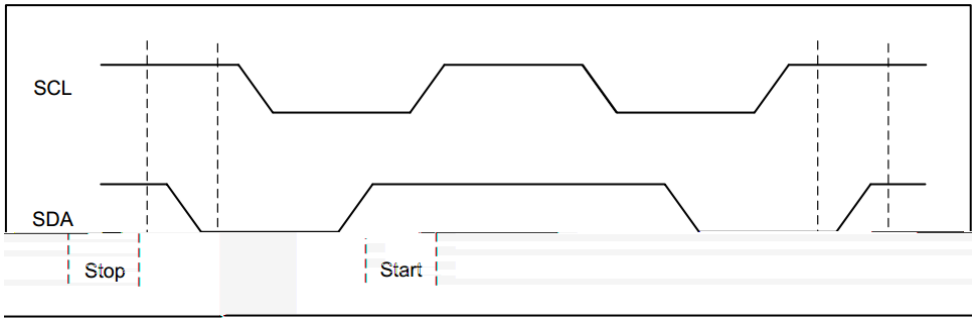


Figure 2 Start and Stop Definition

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BRCM24C04SC BRCM24C04SC “ 0 ”
ACK 9

All addresses and data words are serially transmitted to and from the BRCM24C04SC in 8-bit words. The BRCM24C04SC sends a “0” to acknowledge that it has received each word. This happens during the ninth clock cycle.

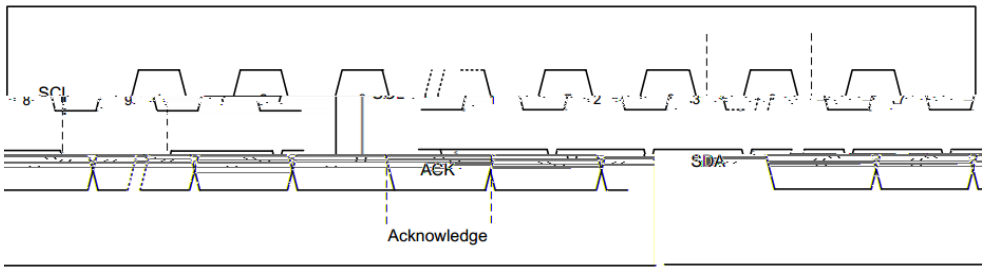


Figure 3 Output Acknowledge

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BRCM24C04SC :(a) ,(b)

| Chip | Access area | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| BRCM24C04SC | Normal Area | 1 | 0 | 1 | 0 | E2 | E1 | P0 | R/W |
| | ID Page | 1 | 0 | 1 | 1 | E2 | E1 | X | R/W |
| | Lock Bit | 1 | 0 | 1 | 1 | E2 | E1 | X | R/W |
| | Serial Number | 1 | 0 | 1 | 1 | E2 | E1 | X | 1 |

Table 1 Device Address

| Chip | Access area | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| BRCM24C04SC | Normal Area | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |
| | ID Page | 0 | 0 | A5 | A4 | A3 | A2 | A1 | A0 |
| | Lock Bit | X | 1 | X | X | X | X | X | X |
| | Serial Number | 1 | 0 | A5 | A4 | A3 | A2 | A1 | A0 |

Table 2 Word Address

E2 E1 4 E2 E1

8 /

0 1 0

The E2, E1 device address bits to allow as many as 4 devices on the same bus. These bits must compare to their corresponding hardwired input pins. The E2, E1 pins use an internal proprietary circuit that biases them to a logic low condition if the pins are floating. The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low. Upon a compare of the device address, the Chip will output a zero. If a compare is not made, the device will return to a standby state.

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BRCM24C04SC WCB Vcc

BRCM24C04SC has a hardware data protection scheme that allows the user to write protect the whole memory when the WCB pin is at Vcc.

p

8

BRCM24C04SC “ 0 ” 8 8

BRCM24C04SC “ 0 ”

BRCM24C04SC BRCM24C04SC

( 5 )

A write operation requires one 8-bit data word address following the device address word and acknowledgment. Upon receipt of this address, the BRCM24C04SC will again respond with a “0” and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the BRCM24C04SC will output a “0” and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. And then the BRCM24C04SC enters an internally timed write cycle, all inputs are disabled during this write cycle and the BRCM24C04SC will not respond until the write is complete (see Figure 5).

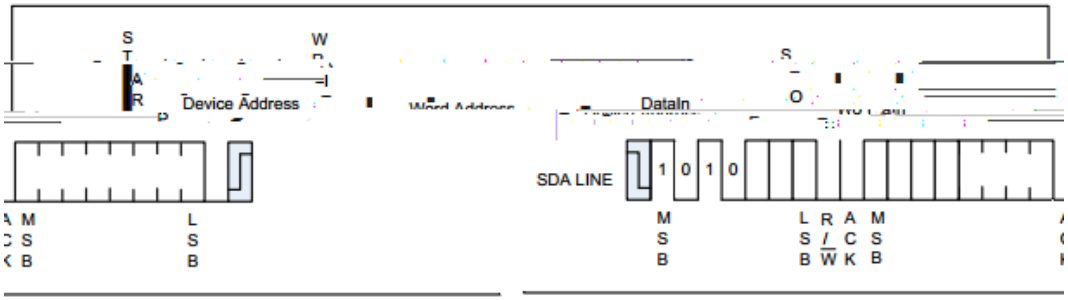


Figure 5 Byte Write

p

BRCM24C04SC BRCM24C04SC

“ 0 ”

A page write is initiated the same as a byte write, but the master does not send a stop condition after the first data word is clocked in. Instead, after the BRCM24C04SC acknowledges receipt of the first data word, the master can transmit more data words. The BRCM24C04SC will respond with a “0” after each data word received. The microcontroller must terminate the page write sequence with a stop condition.

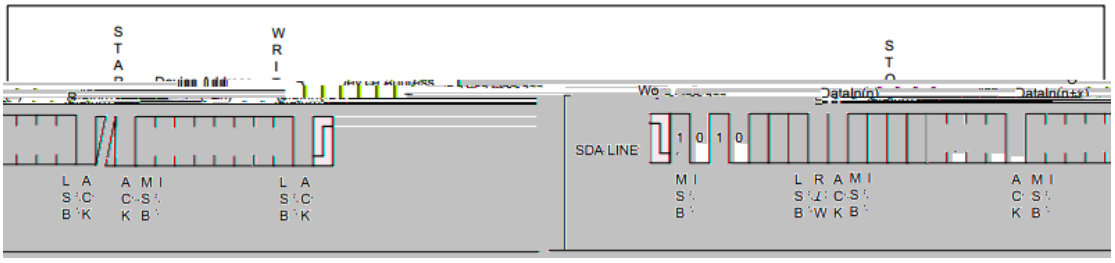


Figure 6 Page Write

4

BRCM24C04SC 16

pr

p

BRCM24C04SC

/ BRCM24C04SC

“ 0 ”

Once the internally timed write cycle has started and the BRCM24C04SC inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the BRCM24C04SC respond with a “0”, allowing the read or write sequence to continue.

p

16

(a) 1011b

(b) A5 / A4 0 1 A7 / A6 “ 00 ”

(c) A3 / A0

NoACK

The Identification Page (16 bytes) is an additional page which can be written and (later) permanently locked in Read-only mode. It is written by the Write Identification Page instruction. This instruction uses the same protocol and format as Page Write (into memory array), except for the following differences:

(a)Device type identifier = 1011b.

(b)Address bits A5/A4 are don’t care while address bit A7/A6 which must be ‘00’.

(c)Address bits A3/A0 define the byte address inside the Identification page. If the Identification page is locked, the data bytes transferred during the Write Identification Page instruction are not acknowledged (NoACK).

p

ID Lock ID

(a) 1011b;

(b) A6 1 ;

(c) xxxx xx1x x 0 1

The Lock Identification Page instruction (Lock ID) permanently locks the Identification page in Read-only mode. The Lock ID instruction is similar to Byte Write (into memory array) with the following specific conditions:

(a)Device type identifier = 1011b.

(b)Address bit A6 must be ‘1’ all other address bits are don’t care.

(c)The data byte must be equal to the binary value xxxx xx1x, where x is don’t care.

p

/ / “ 1 ”

;

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to “1”. There are three read operations: Current Address Read; Random Address Read and Sequential Read.

p

1

/ “ 1 ” BRCM24C04SC

“ 0 ” 7

The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address roll-over during read is from the last byte of the last memory page to the first byte of the first page. Once the device address with the read/write select bit set to “1” is clocked in and acknowledged by the BRCM24C04SC, the current address data word is serially clocked out. The microcontroller does not respond with an input “0” but does generate a following stop condition (see Figure7).

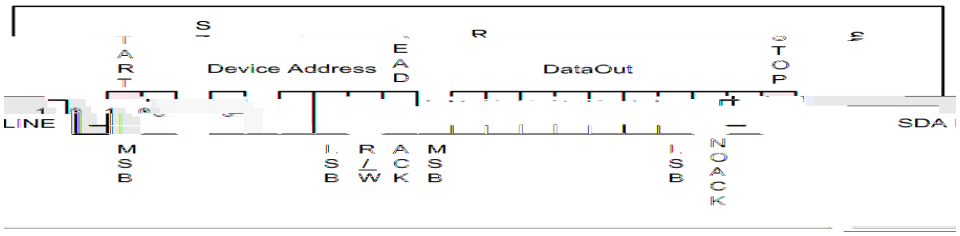


Figure 7 Current Address Read

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“ ”

BRCM24C04SC /

BRCM24C04SC

“ 0 ” 8

A Random Read requires a “dummy” byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the BRCM24C04SC,the microcontroller must generate another start condition. The microcontroller now initiates a Current Address Read by sending a device address with the read/write select bit high. The BRCM24C04SC acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a “0” but does generate a following stop condition (see Figure 8).

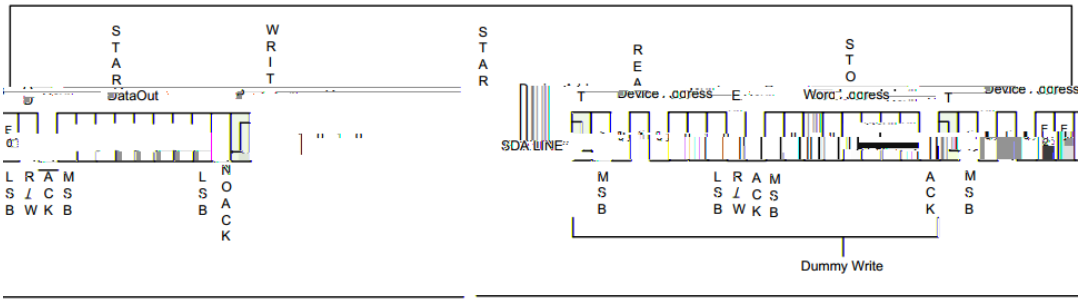


Figure 8 Random Address Read

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BRCM24C04SC

“ 0 ”

9

Sequential Reads are initiated by either a Current Address Read or a Random Address Read. After the microcontroller receives a data word, it responds with acknowledge. As long as the BRCM24C04SC receives acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will roll-over and the Sequential Read will continue. The Sequential Read operation is terminated when the microcontroller does not respond with a “0” but does generate a following stop condition (see Figure 9).

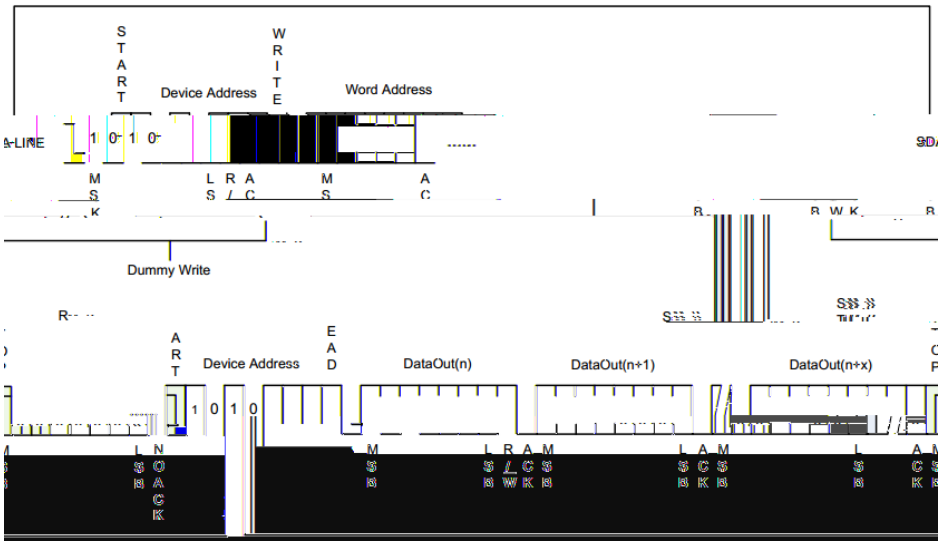



Figure 9 Sequential Read

A7 A6 “ 10 ” 2 “ 10 ”

80h

128 16

128 ACK

7

The Identification Page (16 bytes) is an additional page which can be written and (later) permanently locked in Read-only mode.

Reading the serial number is similar to the sequential read sequence but requires use of the device address seen in Table 1 on page 9, a dummy write, and the use of a specific word address. The entire 128-bit value must be read from the starting address of the serial number block to guarantee a unique number.

Since the address pointer of the device is shared between the regular EEPROM array and the serial number block, a dummy write sequence, as part of a Random Read or Sequential Read protocol, should be performed to ensure the address pointer is set to zero. A Current Address Read of the serial number block is supported but if the previous operation was to the EEPROM array, the address pointer will retain the last location accessed, incremented by one. Reading the serial number from a location other than the first address of the block will not result in a unique serial number.

Additionally, the word address contains a „10□ sequence in bit A7 and A6 of the word address, regardless of the intended address as depicted in Table 2 on page 9. If a word address other than „10□ is used, then the device will output undefined data.

Example: If the application desires to read the first byte of the serial number, the word address input would need to be 80h.

When the end of the 128-bit serial number is reached (16 bytes of data), continued reading of the extended memory region will result in repeated serial number data readout for the data word address will roll-over back to the beginning of the 128-bit serial number. The Serial Number Read operation is terminated when the microcontroller does not respond with a zero (ACK) and instead issues a Stop condition (see Figure 11)

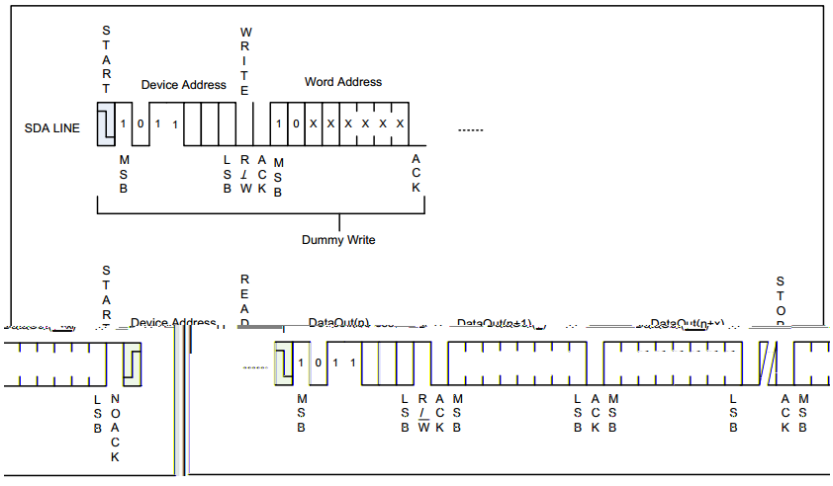
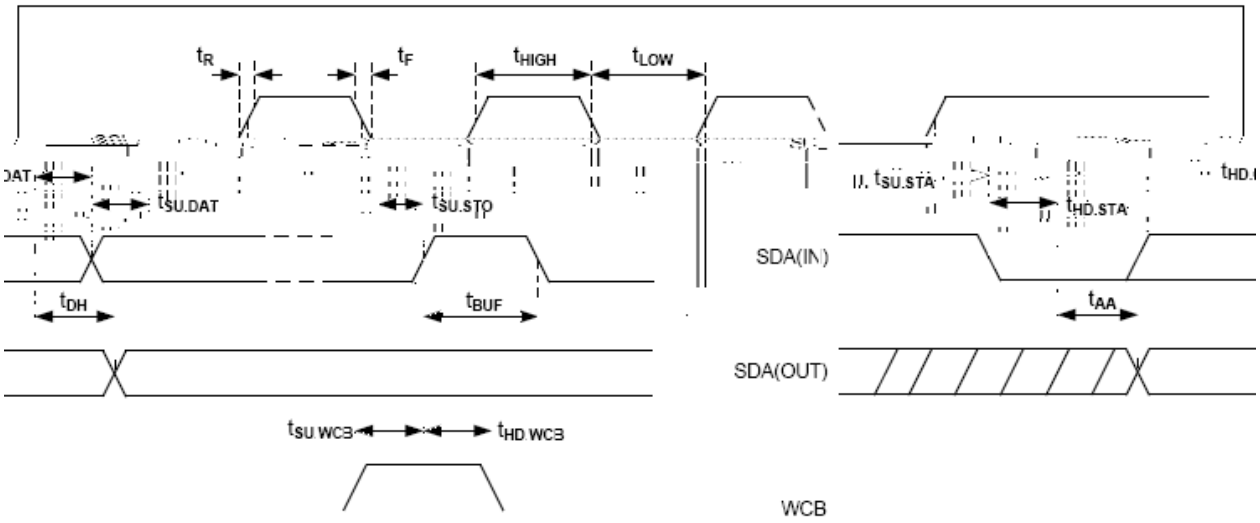
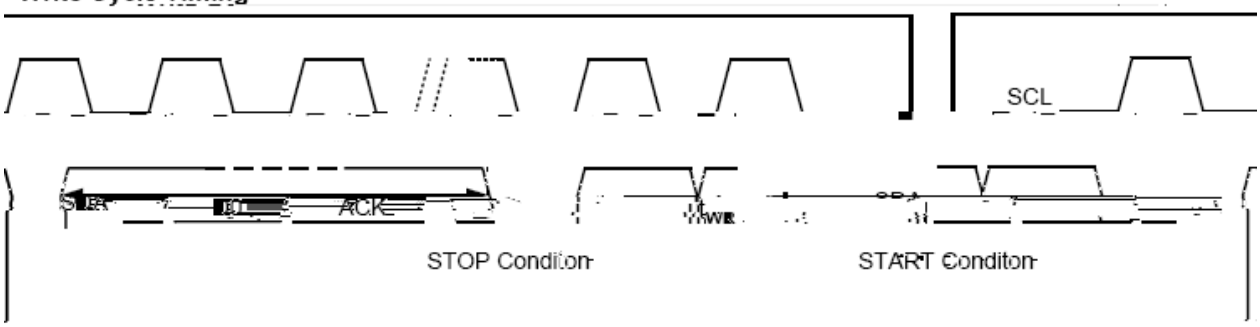



Figure 11 Sequential Read

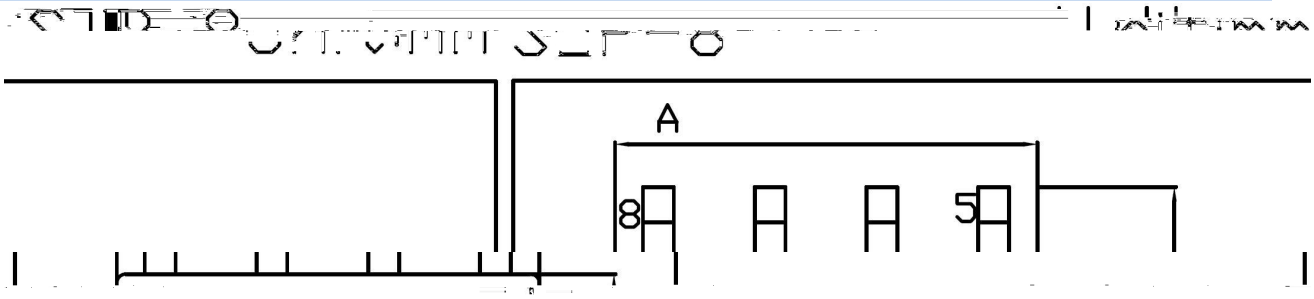
**Bus Timing**

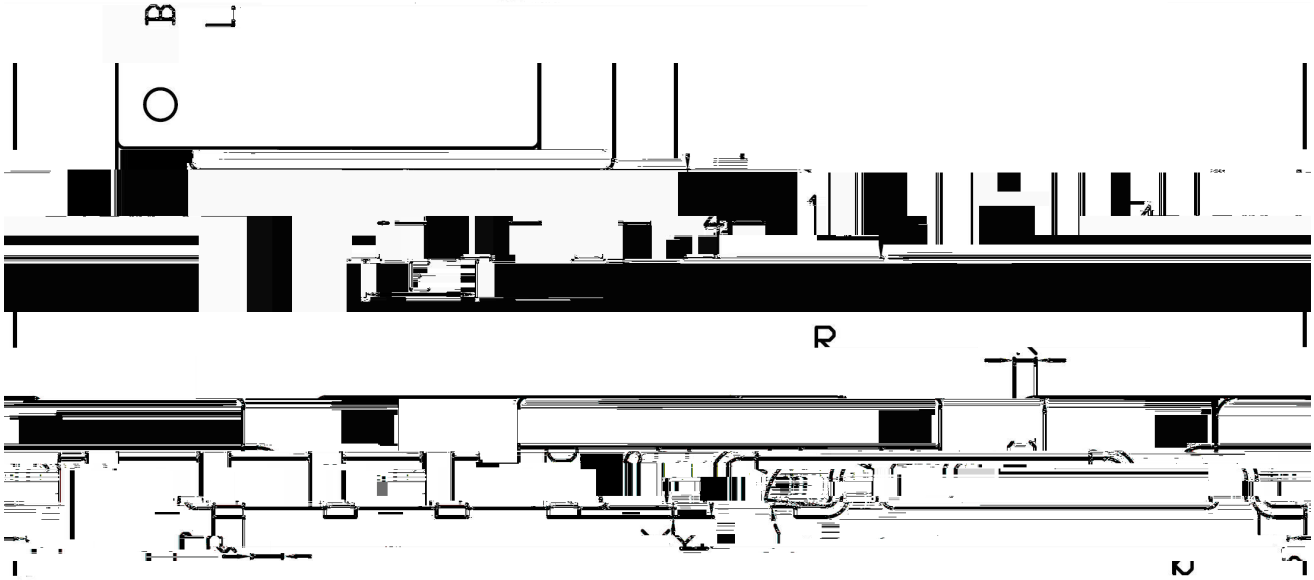


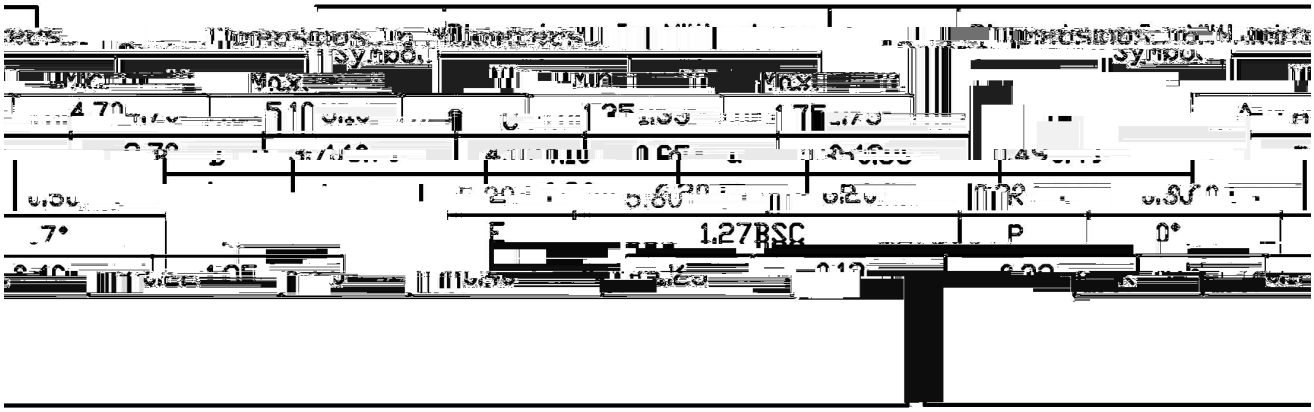

**Write Cycle Timing**

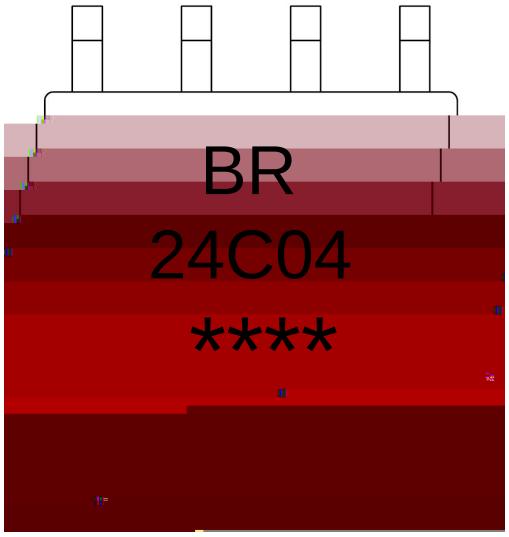



Note: The write cycle time $t_{WR}$ is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.


A




1.27BSC




BR

24C04

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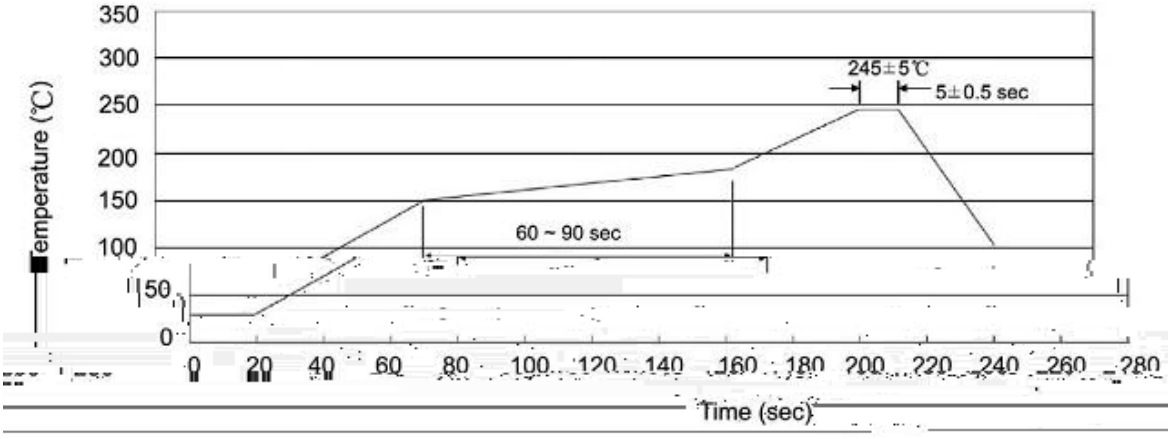
Note:

| | |
|---|---|
| BR: | Company Code. |
| 24C04: | Product Type. |
| ****: | Lot No. Code, code change with Lot No. |




| | | | |
|---|---|---|---|
| | | Note: | |
| 1 | 150 180 60 90sec; | 1.Preheating:150~180 , Time:60~90sec. | |
| 2 | 245±5 5±0.5sec; | 2.Peak Temp.:245±5 , Duration:5±0.5sec. | |
| 3 | 2 10 /sec. | 3. Cooling Speed: 2~10 /sec. | |

260±5 10±1 sec. Temp.:260±5 Time:10±1 sec

/ REEL

| Package Type 封装形式 | Units 包装数量 | | | | | Dimension 包装尺寸 (unit: $mm^3$) | | |
|---|---|---|---|---|---|---|---|---|
| | Units/Reel 只/卷盘 | Reels/Inner Box 卷盘/盒 | Units/Inner Box 只/盒 | Inner Boxes/Outer Box 盒/箱 | Units/Outer Box 只/箱 | Reel | Inner Box 盒 | Outer Box 箱 |
| SOP/ESOP-8 | 4,000 | 2 | 8,000 | 6 | 48,000 | 13 ρ ×12 | 360×360×50 | 380×335×366 |